

ABSTRACT

[0038] A floating-gate transistor for an integrated circuit is formed on a p-type substrate. An n-type region is disposed over the p-type substrate. A p-type region is disposed over the n-type region. Spaced apart n-type source and drain regions are disposed in the p-type region forming a channel therein. A floating gate is disposed above and insulated from the channel. A control gate is disposed above and insulated from the floating gate. An isolation trench disposed in the p-type region and surrounding the source and drain regions, the isolation trench extending down into the n-type region. The substrate, the n-type region and the p-type region each biased such that the p-type region is fully depleted.